UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,892	09/28/2000	Kenneth W. Batcher	72255/06073	7230

23380 7590 02/12/2004

TUCKER, ELLIS & WEST LLP
1150 HUNTINGTON BUILDING
925 EUCLID AVENUE
CLEVELAND, OH 44115-1475

EXAMINER	
OSMAN, AHMED A	
ART UNIT	**PAPER NUMBER**
2136	7

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,892	BATCHER, KENNETH W.	
	Examiner	Art Unit	
	Ahmed A Osman	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED OFFICE ACTION

1. Claims 1 – 15 are presented for examinations.

Drawings

2. New corrected drawings are required in this application because some of the figures contain material that is not legible. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,549,622 to Matthews in view of US Patent No. 6,292,403 to Pancholy.

As per claims 1-12:

Applicant states that the purpose of the claimed invention is to accelerate data processing operations and improve processing speed and efficiency when implementing the RC4 encryption/decryption algorithm (Page 13 Line 2). The office interprets the applicant claims to read as follows. A recurring cycle that involves read/write functions from and to a controller and a memory device in one clock cycle. The clock cycle is divided in 2 halves and 2 events occur in each half of the cycle. It is known to one ordinarily skilled in the art that a clock cycle has a rising edge and a falling edge. Applicant does not specify which events are triggered by the rising edge and which events are triggered by the falling edge. Applicant's invention comprises 2 latches also known as registers in the art. When reading and writing to the registers, the applicant uses the terms "open" and "close" to refer to enabling the reading and writing to the registers. Matthews teaches a system and method for a fast hardware implementation of the RC4 encryption/decryption algorithm. Matthews teaches a method where hardware implementation of the RC4 encryption/decryption algorithm is made faster by reducing the number of cycles needed to perform the encryption/decryption (Column 2 Line 59). Matthews further teaches a method supports a reduction in the number of cycles counts for performing an encryption or decryption algorithm from a 6 to a 2 cycle core (Column 4 Line 48). Matthews teaches that the disclosed invention comprises two dual port memories that allow for simultaneous reads and writes (Column 7 Line 52). Matthews states that both dual ports memories are coupled to the control logic via a

read data bus, a read address bus, a read control bus, write data bus and write address bus (Column 7 Line 36). Matthews does not specifically disclose that the read/write process is executed during one clock cycle. Pancholy teaches an apparatus and a method for implementing a single-cycle read/write operation. Pancholy teaches a periodic signal which is an oscillating waveform that is configured to control one or more circuit functions as part of read and write operation in a memory (Column 3 Line 22). Pancholy further teaches that the periodic signal may be configured to control data transfer operations in response to a first and second transitions which occur in the same periodic cycle and may be complementary to each other (Column 3 Line 27). Pancholy states that this feature enables the memory to operate in a synchronous manner. Furthermore, Pancholy states that the periodic signal may a clock signal or a periodic control signal such as write enable or output enable (Column 3 Line 33). It is clearly illustrated in Figure 4 of Pancholy the sequence of data transfer events that take place during the read and write operations. In the disclosed example, a 125MHz clock is used with a cycle time of 4ns. Therefore the first half of the cycle starts at t=0ns and the second half starts at t=2ns. Pancholy explains the details of the events that occur in the first half of the clock cycle in Column 7 starting on Line 10 till Line 42. Pancholy also explains the details of the events that occur in the second half of the clock cycle on the following paragraph in Column 7 starting on Line 43 and ending in Column 8 at Line 9. Although Pancholy does not specifically state that this invention is applied to a microcode controller system, Pancholy states that the disclosed invention teaches one

skilled in the art to employ it in virtually any appropriately detailed system, structure or manner (Column 3 Line 8).

The office concludes that it would have been obvious to one ordinarily skilled in the art at the time the invention was made to modify Matthews method to implement the method disclosed by Pancholy to further accelerate the data processing and reduce the number of cycles. One would have been motivated to make such a modification in light of Matthews' teachings that one of ordinary skill in the art would understand that a reduction in the number of cycles greatly increases efficiency and reduces cost (Column 2 Line 62).

5. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,549,622 to Matthews in view of US Patent No. 5,517,657 to Rodgers.

As per claims 13-15:

Applicant states that the purpose of the claimed invention is to accelerate data processing operations and improve processing speed and efficiency when implementing the RC4 encryption/decryption algorithm (Page 13 Line 2). The office interprets the applicant claims to read as follows. A recurring cycle that involves read/write functions from and to a controller and a memory device in one clock cycle. The clock cycle is divided into a plurality of phases and 2 events occur in each phase of the cycle. Applicant's invention comprises 2 latches also known as registers in the art.

When reading and writing to the registers, the applicant uses the terms "open" and "close" to refer to enabling the reading and writing to the registers. Matthews teaches a system and method for a fast hardware implementation of the RC4 encryption/decryption algorithm. Matthews teaches a method where hardware implementation of the RC4 encryption/decryption algorithm is made faster by reducing the number of cycles needed to perform the encryption/decryption (Column 2 Line 59). Matthews further teaches a method supports a reduction in the number of cycles counts for performing an encryption or decryption algorithm from a 6 to a 2 cycle core (Column 4 Line 48). Matthews teaches that the disclosed invention comprises two dual port memories that allow for simultaneous reads and writes (Column 7 Line 52). Matthews states that both dual ports memories are coupled to the control logic via a read data bus, a read address bus, a read control bus, write data bus and write address bus (Column 7 Line 36). Matthews does not specifically state that the read/write processes occur in alternating clock phases. Rodgers teaches a procedure for providing an efficient pipeline for reading and writing information to a multiple ported segment register file in different pipestages (Column 2 Line 54). Rodgers also teaches that the read and write of different pipestages associated with separate instructions may occur within the same clock cycle (Column 2 Line 63). Rodgers further states that the read and write operations occur in alternate clock phases (Column 2 Line 65). Rodgers specifically discloses that the first phase precedes the second phase within a given cycle of a clock signal (Column 3 Line 23). Although Rodgers does not specifically state that this invention is applied to a microcode controller system, Rodgers states that it

would be obvious to one skilled in the art that the invention may be practiced in other methods, procedures, components and circuits (Column 4 Line 32). The office concludes that it would have been obvious to one ordinarily skilled in the art at the time the invention was made to modify Matthews method to implement the method disclosed by Rodgers to further accelerate the data processing and reduce the number of cycles. One would have been motivated to make such a modification in light of Matthews' teachings that one of ordinary skill in the art would understand that a reduction in the number of cycles greatly increases efficiency and reduces cost (Column 2 Line 62).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to data processing and microcode controller systems in general:

U.S. Patent No. 4,128,876 to Ames

U.S. Patent No. 4,245,304 to Porter et al.

U.S. Patent No. 5,691,943 to Yun

U.S. Patent No. 5,694,370 to Yoon

U.S. Patent No. 5,790,838 to Irish et al.

U.S. Patent No. 5,809,309 to Leach et al.

U.S. Patent No. 5,973,989 to Pawlowski

U.S. Patent No. 5,999,458 to Nishimura et al.

U.S. Patent No. 6,044,484 to Chung

U.S. Patent No. 6,128,233 to Yu et al.

U.S. Patent No. 6,268,746 to Potter et al.

U.S. Patent No. 6,333,954 to Hansquine

U.S. Patent No. 6,525,971 to Merritt et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ahmed A Osman whose telephone number is 703-305-8910. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

***

Ahmed Osman

United States Patent & Trademark Office

Patent Examiner – AU 2136

January 22, 2004

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100